REMARKS

I. General

Claims 1-44 are pending in the present application. The issues in the current Office Action are as follows:

- Claims 1-4, 13-14, 16-17, 20-26, 33-34, 36-38 and 40-44 are rejected under 35 U.S.C. § 103(a) as being unpatentable over US 5,761,516 (hereinafter *Rostoker*), US 7,079,386 (hereinafter *Jochym*) and US 2003/0088800 (hereinafter *Cai*) in view of what is old and well known in the art.

- Claims 5-7, 18-19, 27-31, 35 and 39 are rejected on the ground of nonstatutory obviousness-type double patenting as being unpatentable over claims 1-9 of US 7,072,185 (hereinafter *Belady*) in view of *Rostoker*, *Jochym*, and *Cai* as applied to claims 1-4, 16-17, 20-26, 33-34, 36-38 and 40-44, and US 5,805,915 (hereinafter *Wilkinson*), and what is old and well known in the art.

- Claims 8-12, 15 and 32 are objected to.

Applicant hereby traverses the rejections and requests reconsideration and withdrawal in light of the remarks contained herein.

II. Claim Objections

On page 14, claims 8-12, 15 and 32 are objected to as being dependent upon a rejected based claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. Applicant thanks the Examiner for this indication of allowable subject matter.

III. Claim Amendments

Claims 27 and 29 are amended to recite, in part, "a processor board." However, the amendment does not exclude other processor boards from the recited system. The amendment

does not narrow the scope of the claim, nor is it made in light of any cited art. Support may be found at least at FIGURES 4A and B and their accompanying descriptions.

Claim 36 is amended to recite, in part, "said cache control and bus bridge device is adapted to exchange data between the processors and a plurality of system components adapted to communicate with a single processor module such that the system components communicate with the plurality of processors as if the system components were communicating with a single-processor module." Support may be found, at least, at [0028] of the specification.

Claim 45 is new. Support may be found at least at FIGURE 1 and its accompanying description. Claim 45 is allowable at least because it depends from claim 27, which is allowable, as described below.

Claim 46 is new. Support may be found at least at FIGURE 3 and its accompanying description. Claim 46 is allowable at least because it depends from claim 1, which is allowable, as described below.

Claim 47 is new. Support may be found, at least, at [0028] of the specification. Claim 47 is allowable at least because it depends from claim 33, which is allowable, as described below.

IV. Claim Rejections

A. Rejection over *Rostoker*, *Jochym*, and *Cai*

On pages 3-11, claims 1-4, 13-14, 16-17, 20-26, 33-34, 36-38 and 40-44 are rejected under 35 U.S.C. § 103(a) as being unpatentable over *Rostoker*, *Jochym* and *Cai* in view of what is old and well known in the art. As an initial matter, it appears that claims 27-31 are not rejected under 35 U.S.C. § 103(a), even though claim 27 is briefly mentioned on page 4 of the Office Action. It is believed that the mention of claim 27 on page 4 is a mistake and that claims 27-31 are rejected only for double patenting.

The test for non-obvious subject matter is whether the differences between the subject matter and the prior art are such that the claimed subject matter as a whole would have been

obvious to a person having ordinary skill in the art to which the subject matter pertains. The United States Supreme Court in Graham v. John Deere and Co., 383 U.S. 1 (1966) set forth the factual inquiries which must be considered in applying the statutory test: (1) determining of the scope and content of the prior art; (2) ascertaining the differences between the prior art and the claims at issue; and (3) resolving the level of ordinary skill in the pertinent art. As discussed further hereafter, Applicant respectfully asserts that the claims include non-obvious differences over the cited art. Applicant asks the Office to reconsider the arguments submitted in the response mailed May 25, 2007. Applicant presents the following additional reasons why the rejections should be withdrawn.

The rejections of independent claims 1, 16, 33, 36, and 41 seem to assert that all of the recited features therein can be found in *Rostoker*. Thus, it appears that the Examiner is rejecting those independent claims under 35 U.S.C. §102, rather than under 35 U.S.C. §103. For example, the rejections fail to explain any differences between the cited art (*Rostoker*) and the independent claims and also fail to explain why one of ordinary skill in the art would modify the *Rostoker* reference to show that any of the independent claims are obvious. Therefore, Applicant respectfully requests that these issues be discussed in the next Office Action or the claims be allowed. Additionally, the claims recite features that are not taught or suggested by the cited portions of the art.

For instance, claim 1 recites, in part, "a cache control and bus bridge device in communication with the plurality of processors such that it is logically interposed between the processors and the system bus." *Rostoker* does not teach or suggest this feature of claim 1. For instance, the Office Action cites items 54 and 56 of FIGURE 2 of *Rostoker* to show the claimed processors, bus 62 to show the claimed system bus, and items 58 and 60 to teach the claimed cache control and bus bridge device. Without admitting that the Office Action's characterization of such components is correct, it is noted that claim 1 recites a different arrangement than that shown in FIGURE 2 of *Rostoker*. Claim 1 recites that the cache control and bus bridge device is "logically interposed between the processors and the system bus." By contrast, items 58 and 60 of *Rostoker* are not interposed between items 54/56 and bus 62. For at least this reason, it is believed that the above-recited feature is not taught by *Rostoker*. The Office Action does not

rely on any of the other references to teach or suggest this feature. Therefore, it is believed that the cited combination does not teach or suggest at least this feature of claim 1.

Further, *Rostoker* fails to disclose at least "wherein the processors and cache control and bus bridge device are disposed in a module form factor such that the apparatus is a drop-in replacement for a standard single-processor module", as recited by claim 1. *Rostoker* appears to be directed to forming a plurality of processors on a single integrated circuit chip together with a memory controller and an I/O controller, *see* Abstract of *Rostoker*. However, *Rostoker* fails to provide any teaching or suggestion of disposing such elements in a module form factor such that the apparatus is a drop-in replacement for a standard single-processor module. The Office Action cites column 3, lines 4-52, of *Rostoker* to teach the feature. The cited passage appears to describe the architecture of *Rostoker*'s FIGURE 2, but the passage does not teach a module conforming to a standard single-processor module form factor. The Office Action does not rely on any of the other references to teach or suggest these features. Therefore, it is believed that the cited combination does not teach or suggest at least these features of claim 1.

Claim 16 recites, in part, "connecting on a local bus a plurality of processors," and "logically interposing between the local bus and a system bus an in-line cache control and bus bridge device." *Rostoker* does not teach or suggest these features of claim 16. For instance, the Office Action cites items 54 and 56 of FIGURE 2 of *Rostoker* to show the claimed processors, bus 62 to show the claimed system bus, and items 58 and 60 to teach the claimed cache control and bus bridge device. Without admitting that the Office Action's characterization of such components is correct, it is noted that claim 16 recites a different arrangement than that shown in FIGURE 2 of *Rostoker*. Claim 16 recites that the cache control and bus bridge device is logically interposed between the local bus and the system bus and that the processors are connected on the local bus. By contrast, items 58 and 60 of *Rostoker* are not interposed between a local bus and bus 62. For at least this reason, it is believed that the above-recited feature is not taught by *Rostoker*. The Office Action does not rely on any of the other references to teach or suggest this feature. Therefore, it is believed that the cited combination does not teach or suggest at least this feature of claim 16.

Further, *Rostoker* fails to disclose at least "disposing in a module conforming to a standard single-processor module form factor the plurality of processors, the local bus, and the in-line cache control and bus bridge device", as recited by claim 16. *Rostoker* appears to be directed to forming a plurality of processors on a single integrated circuit chip together with a memory controller and an I/O controller, *see* Abstract of *Rostoker*. However, *Rostoker* fails to provide any teaching or suggestion of disposing such elements in a module conforming to a standard single-processor module form factor. The Office Action cites column 3, lines 4-52, of *Rostoker* to teach the feature. The cited passage appears to describe the architecture of *Rostoker*'s FIGURE 2, but the passage does not teach a module conforming to a standard single-processor module form factor. The Office Action does not rely on any of the other references to teach or suggest this feature. Therefore, it is believed that the cited combination does not teach or suggest at least this feature of claim 16.

Claim 33 recites, in part, "a cache control and bus bridge device in communication with the plurality of processors such that it is logically interposed between the processors and the system bus." *Rostoker* does not teach or suggest this feature of claim 33. For instance, the Office Action cites items 54 and 56 of FIGURE 2 of *Rostoker* to show the claimed processors, bus 62 to show the claimed system bus, and items 58 and 60 to teach the claimed cache control and bus bridge device. Without admitting that the Office Action's characterization of such components is correct, it is noted that claim 33 recites a different arrangement than that shown in FIGURE 2 of *Rostoker*. Claim 33 recites that the cache control and bus bridge device is "logically interposed between the processors and the system bus." By contrast, items 58 and 60 of *Rostoker* are not interposed between items 54/56 and bus 62. For at least this reason, it is believed that the above-recited feature is not taught by *Rostoker*. The Office Action does not rely on any of the other references to teach or suggest this feature. Therefore, it is believed that the cited combination does not teach or suggest at least this feature of claim 33.

Further, *Rostoker* fails to disclose at least "wherein the processors and cache control and bus bridge device are disposed in a module that is compatible with a single-processor module interface", as recited by claim 33. *Rostoker* appears to be directed to forming a plurality of processors on a single integrated circuit chip together with a memory controller and an I/O

controller, *see* Abstract of *Rostoker*. However, *Rostoker* fails to provide any teaching or suggestion of disposing such elements in a module that is compatible with a single-processor module interface. The Office Action cites column 3, lines 4-52, of *Rostoker* to teach the feature. The cited passage appears to describe the architecture of *Rostoker*'s FIGURE 2, but the passage does not teach a module that is compatible with a single-processor module interface. The Office Action does not rely on any of the other references to teach or suggest these features. Therefore, it is believed that the cited combination does not teach or suggest at least these features of claim 33.

Claim 36 recites, in part, "said cache control and bus bridge device is adapted to exchange data between the processors and a plurality of system components adapted to communicate with a single processor module such that the system components communicate with the plurality of processors as if the system components were communicating with a single-processor module." A similar feature appears in dependent claim 44, which appears to be rejected over only *Rostoker*. *Rostoker* does not teach or suggest this feature of claim 36. The Office Action does not rely on any of the other references to teach or suggest this feature. Therefore, it is believed that the cited combination does not teach or suggest at least this feature of claim 46.

Rostoker fails to disclose at least "means for connecting a module to a system board through an interface compatible with a standard single-processor module", as recited by claim 41. *Rostoker* appears to be directed to forming a plurality of processors on a single integrated circuit chip together with a memory controller and an I/O controller, *see* Abstract of *Rostoker*. However, *Rostoker* fails to provide any teaching or suggestion of disposing such elements in a module that is compatible with a single-processor module interface. The Office Action cites column 3, lines 4-52, of *Rostoker* to teach the feature. The cited passage appears to describe the architecture of *Rostoker*'s FIGURE 2, but the passage does not teach a module that is compatible with a single-processor module interface. The Office Action does not rely on any of the other references to teach or suggest these features. Therefore, it is believed that the cited combination does not teach or suggest at least these features of claim 41.

Dependent claims 2-4, 13-14, 17, 20-26, 33, 34, 37, 38, 40, and 42-44 each depend either directly or indirectly from respective independent claims 1, 16, 33, 36, and 41 and, thus, inherit all of the limitations of their respective independent claims. Thus, the cites portions of the art do not teach or suggest all claim limitations of claims 2-4, 13-14, 17, 20-26, 33, 34, 37, 38, 40, and 42-44. It is respectfully submitted that dependent claims 2-4, 13-14, 17, 20-26, 33, 34, 37, 38, 40, and 42-44 are allowable at least because of their dependence from their respective base claims for the reasons discussed above. Accordingly, Applicant respectfully requests the withdrawal of the 35 U.S.C. § 103(a) rejection of claims 1-4, 13-14, 16-17, 20-26, 33-34, 36-38 and 40-44.

B. Double Patenting Rejection

On pages 11-14, claims 5-7, 18-19, 27-31, 35 and 39 are rejected on the ground of nonstatutory obviousness-type double patenting as being unpatentable over claims 1-9 of *Belady* in view of *Rostoker*, *Jochym*, and *Cai* as applied to claims 1-4, 16-17, 20-26, 33-34, 36-38 and 40-44, and *Wilkinson*, and what is old and well known in the art.

Claims 5-7, 18-19, 27-31, 35, and 39 are rejected on the ground of nonstatutory obviousness-type double-patenting as being unpatentable over claims 1-9 of *Belady* in view of *Rostoker* in view of *Jochym* and further in view of *Cai* and further in view of *Wilkinson* and still further in view of what the Examiner alleges to be "old and well known in the art" (hereinafter "*Official Notice*"), *see* Page 4 of Office Action. Applicant respectfully traverses for the reasons stated below.

An obviousness-type double patenting rejection should make clear the differences between the inventions defined by the conflicting claims—a claim in the patent compared to a claim in the application, and the reasons why a person of ordinary skill in the art would conclude that the invention defined in the claim at issue would have been an obvious variation of the invention defined in a claim in the patent. M.P.E.P. § 804(II)(B)(1).

Further, *Belady* is a patent having a filing date later than the filing date of the present application, and thus two-way obviousness must be established, *see* M.P.E.P. § 804(II)(B)(1)(b).

Accordingly, to establish a proper grounds of obviousness-type double patenting, the Examiner must apply the *Graham* obviousness analysis twice, once with the present application's claims as the claims in issue and once with *Belady's* claims as the claims in issue. *Id.*

Claim 1 of *Belady* recites, in part, "a system board with pass-thru holes" and "wherein the thermal dissipation device extends through at least one of the pass-thru holes". No reasoning has been identified regarding why this element of claim 1 of *Belady* would be obvious from the claims of the present application. As noted above, two-way obviousness is required to be established to support the outstanding double-patenting rejection.

Accordingly, Applicant respectfully requests that the Examiner withdraw the obviousness-type double patenting rejection of record.

V. Conclusion

In view of the above, Applicant believes the pending application is in condition for allowance.

Applicant believes a fee of $1,140.00 is due with this response. However, if additional fees are due, please charge our Deposit Account No. 08-2025, under Order No. 200309347-2 from which the undersigned is authorized to draw.

Respectfully submitted,

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I hereby certify that this paper (along with any paper referred to as being attached or enclosed) is being transmitted via the Office electronic filing system in accordance with § 1.6(a)(4).

Dated: October 26, 2007

Signature: _____
(Donna Dobson)